DATA SHEET

SC68C562

CMOS dual universal serial communications controller (CDUSCC)

Product data
Supersedes data of 1998 Sep 04

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Philips
Semiconductors

PHILIPS

CMOS Dual universal serial communications controller (CDUSCC) SC68C562

DESCRIPTION

The Philips Semiconductors SC68C562 Dual Universal Serial Communications Controller (CDUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SC68C562 interfaces to the 68000 MPUs via asynchronous bus control signals and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The SC68C562 is hardware (pin) and software (Register) compatible with SCN68562 (NMOS version). It will automatically configure to NMOS DUSCC register map on power-up or reset.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock.

This makes the CDUSCC well suited for dual speed channel applications. Data rates up to 10 Mb/s are supported.

Each transmitter and each receiver is serviced by a 16-byte FIFO. The receiver FIFO also stores 9 status bits for each character received; the transmit FIFO is able to store transmitter commands with each byte. This permits reading and writing of up to 16 bytes at a time, thus minimizing the potential for transmitter underrun, receiver overrun and reducing interrupt or DMA overhead.

In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full. Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs are general purpose in nature, they can be optionally programmed for other functions. This document contains the electrical specifications for the SC68C562. Refer to the CMOS Dual Universal Serial Communications Controller (CDUSCC) User Manual for a complete operational description of this product.

FEATURES

- Full hardware and software upward compatibility with previous NMOS device

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Low power CMOS process
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Sixteen character receiver and transmitter FIFOs
- 0 to 10 MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 19 fixed rates: 50 to 64 kbaud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with the Philips Semiconductors SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Transmit path clear status
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Interrupt at any FIFO fill level
  - Maskable interrupt conditions
- FIFO'd status bits
- Watchdog timer
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general I/O pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5 V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors

- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 10 Mb/s at 1X and receive up to 1 Mb/s at 16X data rates

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line fill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs line fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

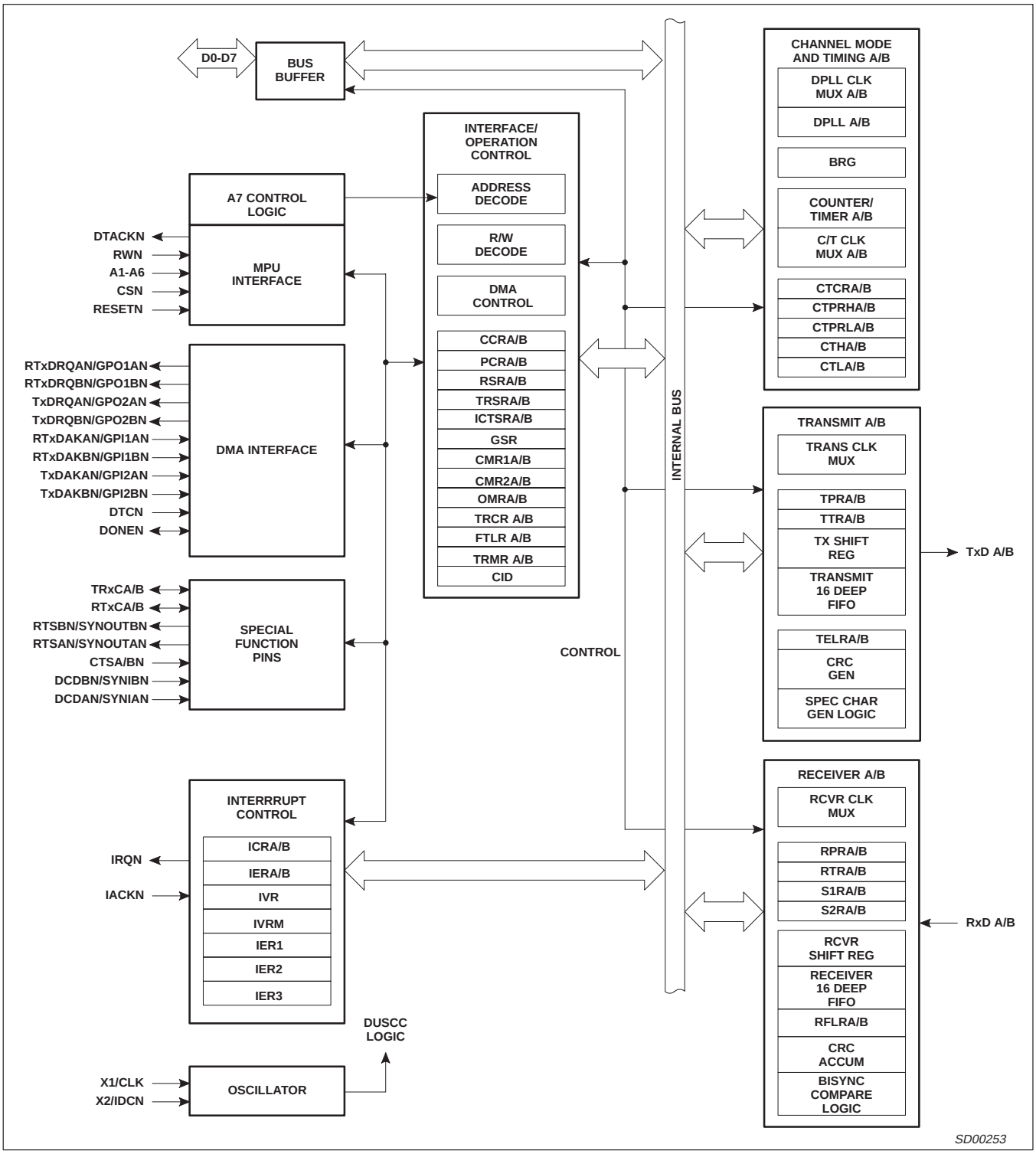
V_{CC} = +5V ± 10 %; T_{amb} = 0 °C to +70 °C. Serial data rate = 10 Mb/s

Type number	Package		
	Name	Description	Version
SC68C562C1A	PLCC52	plastic leaded chip carrier; 52 leads; pedestal	SOT238-3

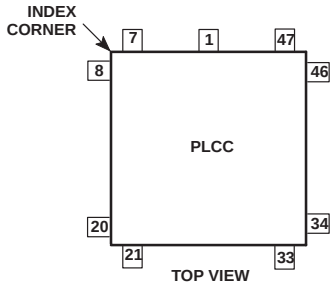
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_{amb}	Operating ambient temperature[2]	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} +0.5	V

BLOCK DIAGRAM



PIN CONFIGURATION



Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/GPI1BN	31	D2
6	IRQN	32	D1
7	NC	33	D0
8	RESETN	34	NC
9	RTSBN/SYNOUTBN	35	CTSAN/LCAN
10	TRxCB	36	TxDRQAN/GPO2AN/RTSAN
11	RTxCB	37	RTxDRQAN/GPO1AN
12	DCDBN/SYNIBN	38	TxDAKAN/GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/GPI2BN	42	DCDAN/SYNIAN
17	RTxDRQBN/GPO1BN	43	RTxCA
18	TxDRQBN/GPO2BN/RTSBN	44	TRxCA
19	CTSBN/LCBN	45	RTSAN/SYNOUTAN
20	D7	46	X2/IDCN
21	D6	47	X1/CLK
22	D5	48	RTxDAKAN/GPI1AN
23	D4	49	A6
24	DTACKN	50	A5
25	DTCN	51	A4
26	GND	52	V_{DD}

SD00739

PIN DESCRIPTION

MNEMONIC	PIN	TYPE	NAME AND FUNCTION
A1–A6	4-2, 51-49	I	**Address Lines:** Active-HIGH. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0–D7	33-30, 23-20	I/O	**Bidirectional Data Bus:** Active-HIGH, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command and status transfers between the CPU and the CDUSCC take place over this bus. The data bus is enabled when CSN and R/WN or during interrupt acknowledge cycles and single address DMA acknowledge cycles.
R/WN	28	I	**Read/Write:** A HIGH input indicates a read cycle and a LOW indicates a write cycle when CEN is active.
CSN	27	I	**Chip Select:** Active-LOW input. When active, data transfers between the CPU and the CDUSCC are enabled on D0–D7 as controlled by R/WN and A1–A6 inputs. When CSN is HIGH, the data lines are placed in the 3-State condition (except during interrupt acknowledge cycles and single address DMA transfers).
IRQN	6	O	**Interrupt Request:** Active-LOW, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the CDUSCC to output an interrupt vector on the data bus.
IACKN	1	I	**Interrupt Acknowledge:** Active-LOW. When IACKN is asserted, the CDUSCC responds by either forcing the bus into high-impedance, placing a vector number, call instruction or zero on the data bus. The vector number can be modified or unmodified by the status. If no interrupt is pending, IACKN is ignored and the data bus placed in high-impedance.
X1/CLK	47	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, an external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals. When a crystal is used, a capacitor must be connected from this pin to ground.

MNEMONIC	PIN	TYPE	NAME AND FUNCTION
X2/IDCN	46	O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide an interrupt daisy chain active-LOW output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be left floating when an external clock is used on X1 and X2 is not used as an interrupt daisy chain output. When a crystal is used, a capacitor must be connected from this pin to ground.
RESETN	8	I	**Master Reset:** Active-LOW. A LOW on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of the CDUSCC Users' Guide. Reset is asynchronous, i.e., no clock is required.
RxDA, RxDB	40, 14	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	39, 15	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is in the marking (HIGH) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	43, 11	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X).
TRxCA, TRxCB	44, 10	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1 ÷ 2).
CTSA/BN, LCA/BN	35, 19	I/O	**Channel A (B) Clear-to-Send Input or Loop Control Output:** Active-LOW. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The CDUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the BOP loop mode, this pin becomes a loop control output which is asserted and negated by CDUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	42, 12	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-LOW input, it acts as an enable for the receiver or can be used as a general purpose input. For the DCD function, the CDUSCC detects logic level transitions on this pin and can be programmed to generate an interrupt when a transition occurs. As an active-LOW external sync input, it is used in COP mode to obtain character synchronization for the receiver without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	37, 17	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-LOW. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	36, 18	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-LOW. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control.
RTxDAKA/BN, GPI1A/BN	48, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-LOW. For half-duplex single address operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO when the receiver is enabled or load transmitter FIFO when the transmitter is enabled) is beginning. For full-duplex single address DMA operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GPI2A/BN	38, 16	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-LOW. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the CDUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.

MNEMONIC	PIN	TYPE	NAME AND FUNCTION
DONEN	29	I/O	**Done:** Active-LOW, open-drain. DONEN can be used and is active in both DMA and non-DMA modes. As an input, DONEN indicates the last DMA transfer cycle to the TxFIFO. As an output, DONEN indicates either the last DMA transfer from the RxFIFO or that the transmitted character count has reached terminal count.
RTSA/BN, SYNOUTA/BN	45, 9	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-LOW. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
DTACKN	24	O	**Data Transfer Acknowledge:** Active-LOW, 3-state. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. In a write bus cycle, input data is latched by the assertion (falling edge) of DTACKN or by the negation (rising edge) of CSN, whichever occurs first. The signal is negated when completion of the cycle is indicated by negation of CSN or IACKN input, and returns to the inactive state (3-state) a short period after it is negated. In single address DMA mode, input data is latched by the assertion (falling edge) of DTCN or by the negation (rising edge) of the DMA acknowledge input, whichever occurs first. DTACK is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-state) a short period after it is negated. When inactive, DTACKN requires an external pull-up resistor.
DTC	25	I	**Device Transfer Complete:** Active-LOW. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
V_{CC}	34, 52	I	**+5V Power Input**
GND	26, 13, 41, 7	I	**Signal and Power Ground Input**

ELECTRICAL CHARACTERISTICS[4, 5]

T_{amb} = 0 °C to +70 °C, V_{CC} = 5.0 V ± 10 %

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input LOW voltage:					
	All except X1/CLK		–	–	0.8	V
	X1/CLK		–	–	0.8	V
V_{IH}	Input HIGH voltage:					
	All except X1/CLK		2.0	–	–	V
	X1/CLK		$0.8 \times V_{CC}$	–	V_{CC}	V
V_{OL}	Output LOW voltage:[14]					
	All except IRQN	I_{OL} = 5.3 mA	–	–	0.5	V
	IRQN[7]	I_{OL} = 8.8 mA	–	–	0.5	V
V_{OH}	Output HIGH voltage:[14] (Except open drain outputs)	I_{OH} = –400 µA	V_{CC} – 0.5	–	–	V
I_{ILX1}	X1/CLK input LOW current[10]	V_{IN} = 0, X2 = GND	–150	–	0.0	µA
I_{IHX1}	X1/CLK input HIGH current[10]	$V_{IN} = V_{CC}$, X2 = GND	–	–	150	µA
I_{SCX2}	X2 short circuit current (X2 mode)	X1 open; V_{IN} = 0 V	–	–	–15	mA
		$V_{IN} = V_{CC}$	–	–	+15	mA
I_{IL}	Input LOW current on RESETN, DTCN, TxDAKA/BN, RTxDAKA/BN	V_{IN} = 0 V	–15	–	–0.5	µA
I_L	Input leakage current	V_{IN} = 0 V to V_{CC}	–1	–	+1	µA
I_{OZH}	Output off current HIGH, 3-State data bus	$V_{IN} = V_{CC}$	–	–	+1	µA
I_{OZL}	Output off current LOW, 3-State data bus	V_{IN} = 0 V	–1	–	–	µA
I_{ODL}	Open drain output LOW current in off state:					
	DONEN, DTACKN (3-state)	V_{IN} = 0 V	–15	–	–0.5	µA
	IRQN	V_{IN} = 0 V	–1	–	–	µA
I_{ODH}[6]	Open drain output HIGH current in off state: DONEN, IRQN, DTACKN (3-state)	$V_{IN} = V_{CC}$	–1	–	+1	µA
I_{CC}	Power supply current[16] (See Figure 17 for graphs)	0 °C to 70 °C	–	25	80	mA
C_{IN}	Input capacitance[9]	V_{CC} = GND = 0 V	–	–	10	pF
C_{OUT}	Output capacitance[9]	V_{CC} = GND = 0 V	–	–	15	pF
$C_{I/O}$	Input/output capacitance[9]	V_{CC} = GND = 0 V	–	–	20	pF

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. Clock may be stopped (DC) for testing purposes or when the CDUSCC is in non-operational modes. Operation down to 0 rate clocks is implied by a full static CMOS design, but is not verified in testing or characterization.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature and voltage range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.2 V and 3.0 V with a transition time of 20 ns maximum. For X1/CLK, this swing is between 0.2 V and 4.4 V. All time measurements are referenced at input voltages of 0.2 V and 3.0 V and output voltages of 0.8 V and 2.0 V, as appropriate.
6. See Figure 18 for test conditions for outputs.
7. Tests for open drain outputs are intended to guarantee switching of the output transistor. To include noise margin this response is measured from the switching signal midpoint to 0.2 V above the required output level.
8. Execution of the valid command (after it is latched) requires a minimum of three rising edges of X1 (see Figure 19).
9. These values were no explicitly tested; they are guaranteed by design and characterization data.
10. X1/CLK and X2 are not tested with a crystal installed.
11. X1/CLK frequency must be at least as fast as the faster of the receiver or transmitter data rate.
12. The X1 clock drives DTACKN, Baud Rate Generator, command register and the update of the FIFO fill level encoders. The Command Register requires three X1 clocks between two commands; FIFO fill level encoding requires 2.5 to 3.5 X1 cycles.
13. The 68562 bus interface may be operated in two modes; a 68000 compatible mode with automatic DTACK generation and a short chip select mode. DTACKN should not be used externally in the short chip select mode. The DTACKN signal is generated by the assertion of the chip select, and data is latched by assertion of DTACKN or by de-assertion of the chip select, whichever comes first. In single address DMA, the DTACK signal will be de-asserted by the assertion of the DTCN or from the de-assertion of the TxDAKN, whichever occurs first.
14. Also includes X2/IDCN pin in IDC mode.
15. In case of 3-state output, output levels V_{OL} + 0.2 V are considered float or high-impedance.
16. V_O = 0 V to V_{CC}, Rx/Tx at 10 MHz and X1 at 10 MHz

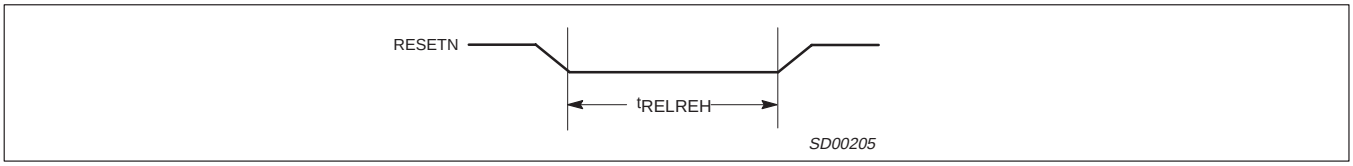


Figure 1. Reset Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RELREH}	RESETN LOW to RESETN HIGH	200	–	ns

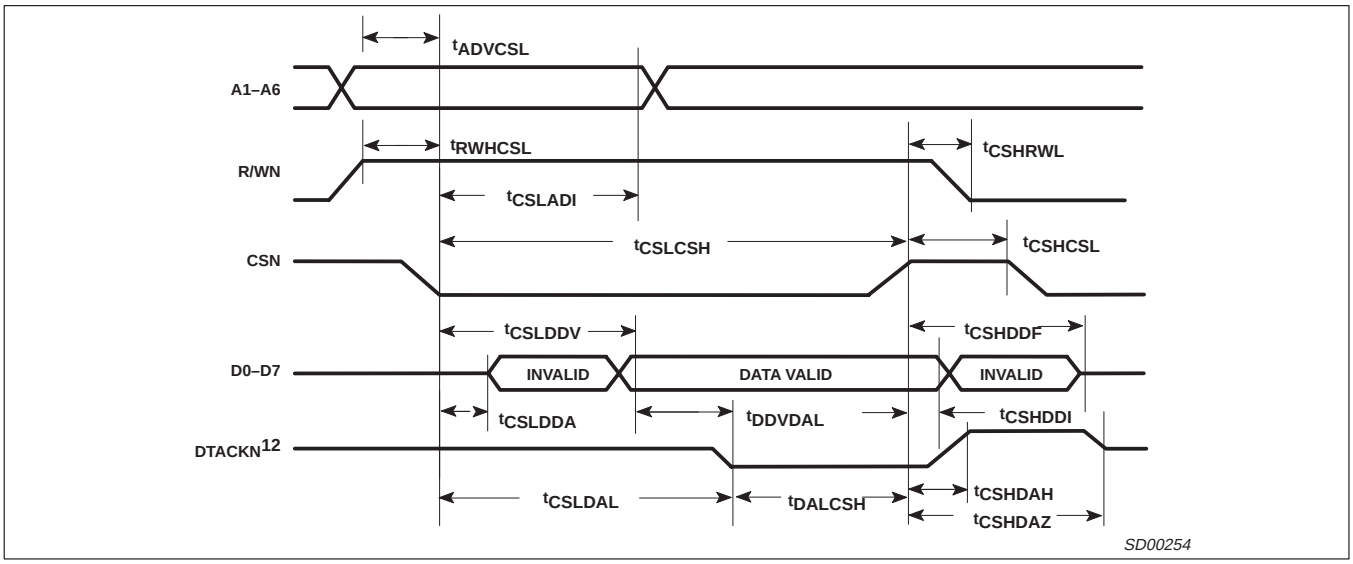


Figure 2. Read Cycle Bus Timing

Times represent an X1 clock frequency of 14.745 MHz				
SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{ADVCSL}	A0-A6 valid to CSN LOW	5	–	ns
t_{RWHCSL}	RWN HIGH to CSN LOW	5	–	ns
t_{CSHRWL}	CSN HIGH to RWN LOW	10	–	ns
t_{CSHCSL}	CSN HIGH to CSN LOW[8]	30	–	ns
t_{CSLDDV}	CSN LOW to read data valid	–	130	ns
t_{CSHDDF}	CSN HIGH to data bus float	–	40	ns
t_{DDVDAL}	Read data valid to DTACKN LOW[9]	20	–	ns
t_{DALCSH}	DTACKN LOW to CSN HIGH[9]	0	–	ns
t_{CSLDAL}[13]	CSN LOW to DTACKN LOW[9]	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{CSHDAH}	CSN HIGH to DTACKN HIGH	–	60	ns
t_{CSHDAZ}	CSN HIGH to DTACKN HIGH impedance	–	90	ns
t_{CSLADI}	CSN LOW to address invalid	50	–	ns
t_{CSLCSH}	CSN LOW to CSN HIGH	130	–	ns
t_{CSLDDA}	CSN LOW to data bus driver active[9]	10	–	ns
t_{CSHDDI}	CSN HIGH to data invalid	5	–	ns

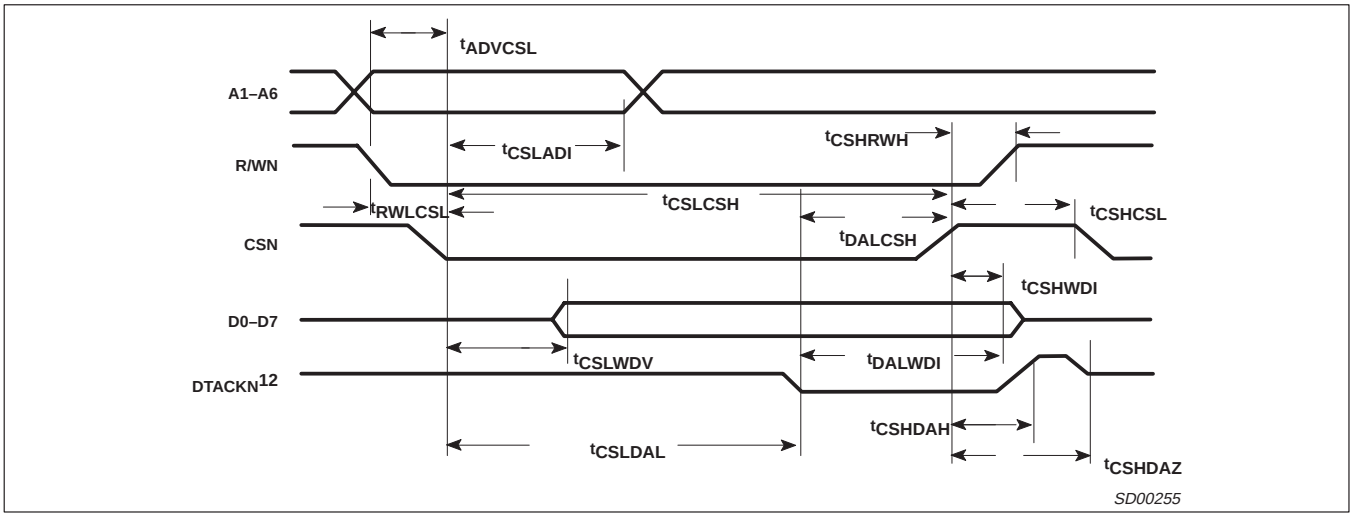


Figure 3. Write Cycle Bus Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{ADVCSL}	A0-A6 valid to CSN LOW	5	–	ns
t_{CSLADI}	CSN LOW to A0-A6 invalid	50	–	ns
t_{RWLCSL}	RWN LOW to CSN LOW	0	–	ns
t_{CSHRWH}	CSN HIGH to RWN HIGH	0	–	ns
t_{CSHCSL}	CSN HIGH to CSN LOW[8]	30	–	ns
t_{DALCSH}	DTACKN LOW to CSN HIGH[9]	0	–	ns
t_{DALWDI}	DTACKN LOW to write data invalid[9]	0	–	ns
t_{CSLDAL}[13]	CSN LOW to DTACKN LOW[9]	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{CSHDAH}	CSN HIGH to DTACKN HIGH	–	60	ns
t_{CSHDAZ}	CSN HIGH to DTACKN high-impedance	–	90	ns
t_{CSLCSH}	CSN LOW to CSN HIGH	130	–	ns
t_{CSLWDV}	CSN LOW to write data valid	35	–	ns
t_{CSHWDI}	CSN HIGH to write data invalid	5	–	ns

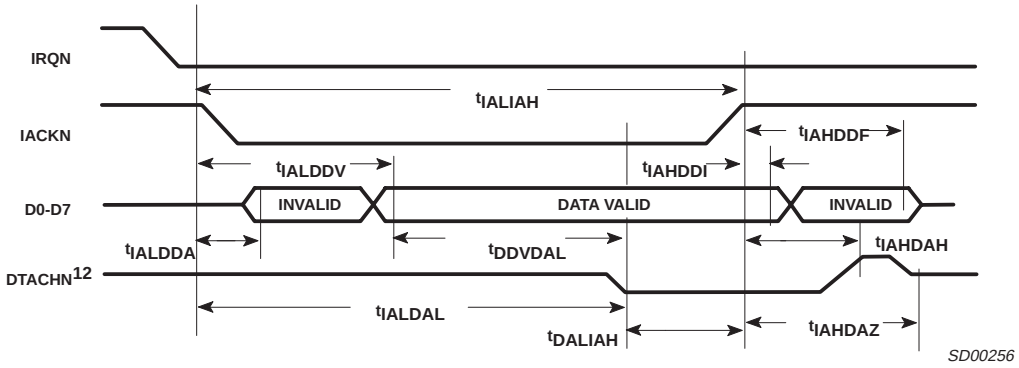


Figure 4. Interrupt Cycle Timing

SYMBOL	PARAMETER[12]	LIMITS		UNIT
		Min	Max	
t_{IALIAH}	IACKN LOW to IACKN HIGH	130	–	ns
t_{IALDDA}	IACKN LOW to data bus drivers active[9]	10	–	ns
t_{IALDDV}	IACKN LOW to read data valid	–	130	ns
t_{IAHDDF}	IACKN HIGH to data bus floating	–	60	ns
t_{DDVDAL}	Read data valid to DTACKN LOW[9]	20	–	ns
t_{IAHDAH}	IACKN HIGH to DTACKN HIGH	–	70	ns
t_{IAHDAZ}	IACKN HIGH to DTACKN high-impedance	–	100	ns
t_{IALDAL}	IACKN LOW to DTACKN LOW[9]	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{IAHDDI}	IACKN HIGH to data bus invalid	5	–	ns
t_{DALIAH}	DTACKN LOW to IACKN HIGH[9]	0	–	ns

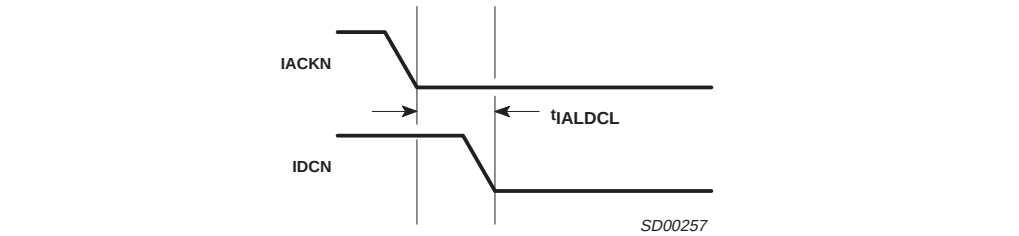


Figure 5. Interrupt Daisy Chain Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{IALDCL}	IACKN LOW to IDCN (daisy chain) LOW	–	60	ns

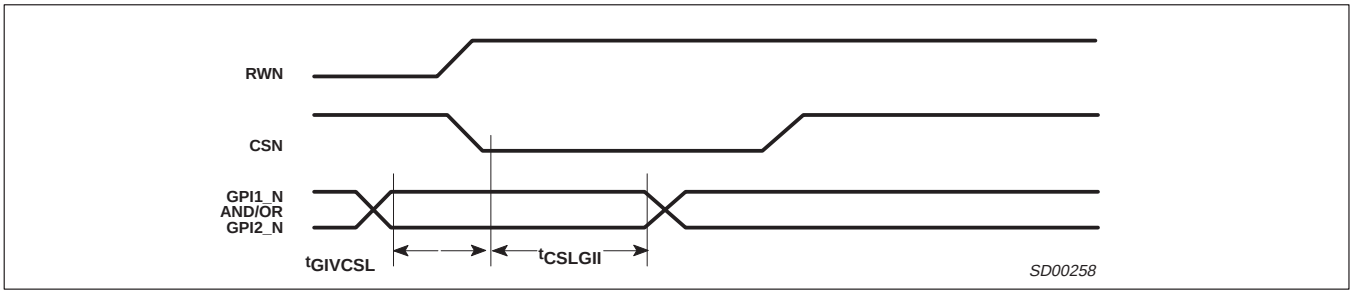


Figure 6. Input Port Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{GIVCSL}	GPI input valid to CSN LOW	20	–	ns
t_{CSLGII}	CSN LOW to GPI input invalid	40	–	ns

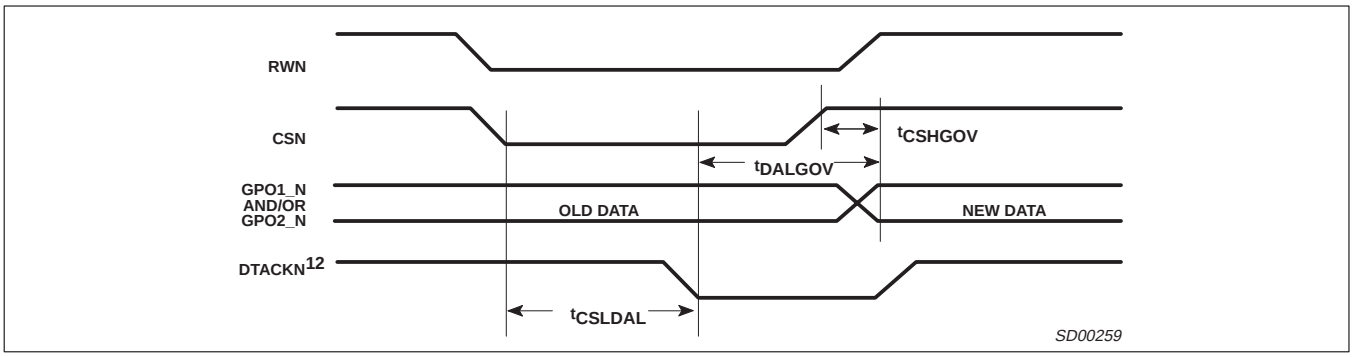


Figure 7. Output Port Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{DALGOV}	DTACKN LOW to GPO output data valid[9]	–	40	ns
t_{CSLDAL}[13]	CSN LOW to DTACKN LOW[9]	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{CSHGOV}	CSN HIGH to GPO output data valid	–	100	ns

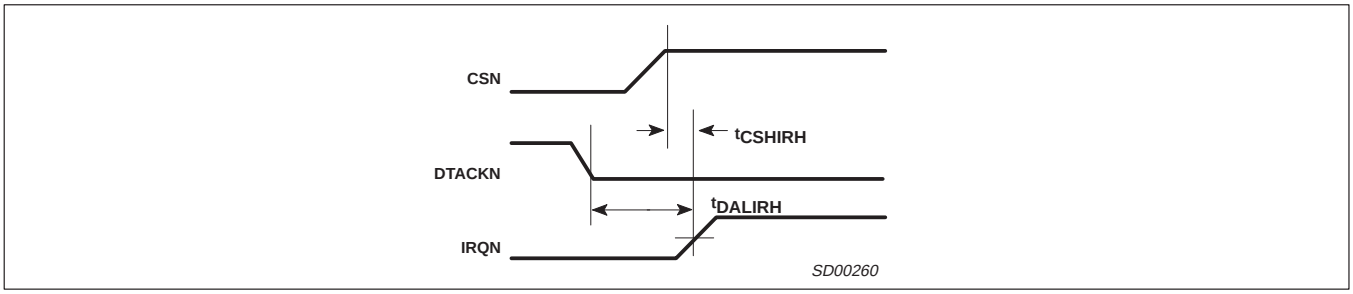


Figure 8. Interrupt Timing, Write Cycle

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{DALIRH}	DTACKN LOW to IRQN HIGH, write cycle[9]			
	Write TxFIFO (TxRDY interrupt)[9]	–	40	ns
	Write RSR (Rx condition interrupt)[9]	–	40	ns
	Write TRSR (Rx/Tx interrupt)[9]	–	40	ns
	Write ICTSR (port change and CT interrupt)[9]	–	40	ns
	Write TRMSR (Tx Path, Patt recognition)[9]	–	40	ns
t_{CSHIRH}	CSN HIGH to IRQN HIGH, write cycle			
	Write TxFIFO (TxRDY interrupt)	–	90	ns
	Write RSR (Rx condition interrupt)	–	90	ns
	Write TRSR (Rx/Tx interrupt)	–	90	ns
	Write ICTSR (port change and CT interrupt)	–	90	ns
	Write TRMSR (Tx Path, Patt recognition)[9]	–	90	ns

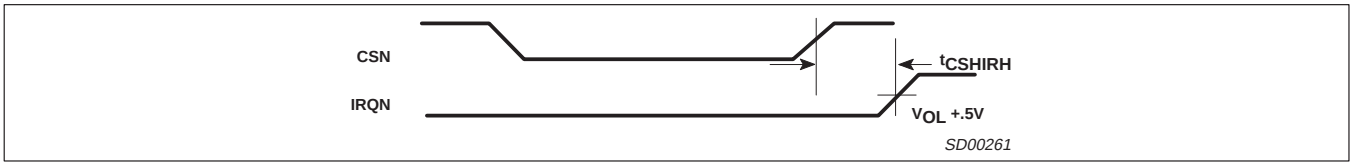


Figure 9. Interrupt Timing, Read Cycle

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{CSHIRH}	CSN HIGH to IRQN HIGH, read cycle			
	Read RxFIFO (RxRDY interrupt)	–	90	ns

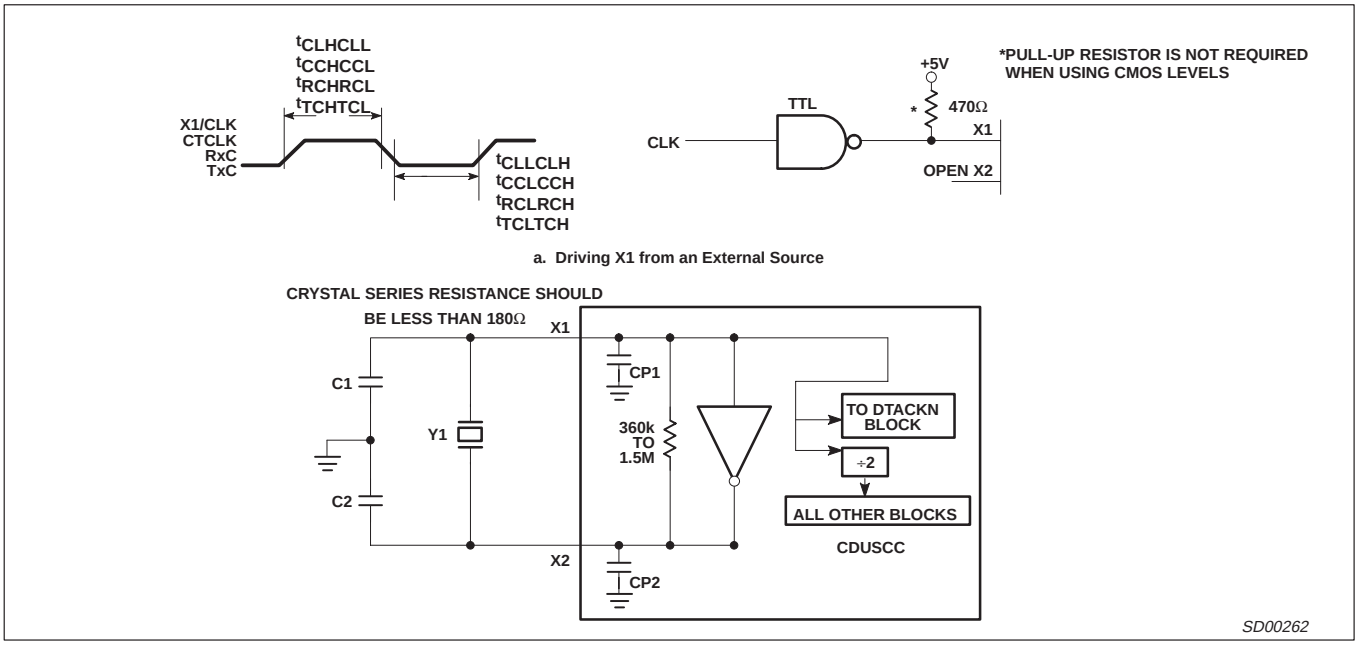


Figure 10. Receive, Dual Address DMA

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{CLHCLL}	X1/CLK HIGH to LOW time	25	–	–	ns
t_{CLLCLH}	X1/CLK LOW to HIGH time	25	–	–	ns
t_{CCHCCL}	CT and DPLL CLK HIGH to LOW time	45	–	–	ns
t_{CCLCCH}	CT and DPLL CLK LOW to HIGH time	45	–	–	ns
t_{RCHRCL}	RxC HIGH to LOW time	50	–	–	ns
t_{RCLRCH}	RxC LOW to HIGH time	50	–	–	ns
t_{TCHTCL}	TxC HIGH to LOW time	50	–	–	ns
t_{TCLTCH}	TxC LOW to HIGH time	50	–	–	ns
f_{CL}	X1/CLK frequency[11, 2]	0	14.7456	16.0	MHz
f_{CC}	CT CLK frequency	0	–	10	MHz
f_{RC}	RxC frequency (16X or 1X)	0	–	10	MHz
f_{TC}	TxC frequency (16X or 1X)	0	–	10	MHz
f_{RTC}	Tx/Rx frequency for FM/Manchester encoding	–	–	5	MHz

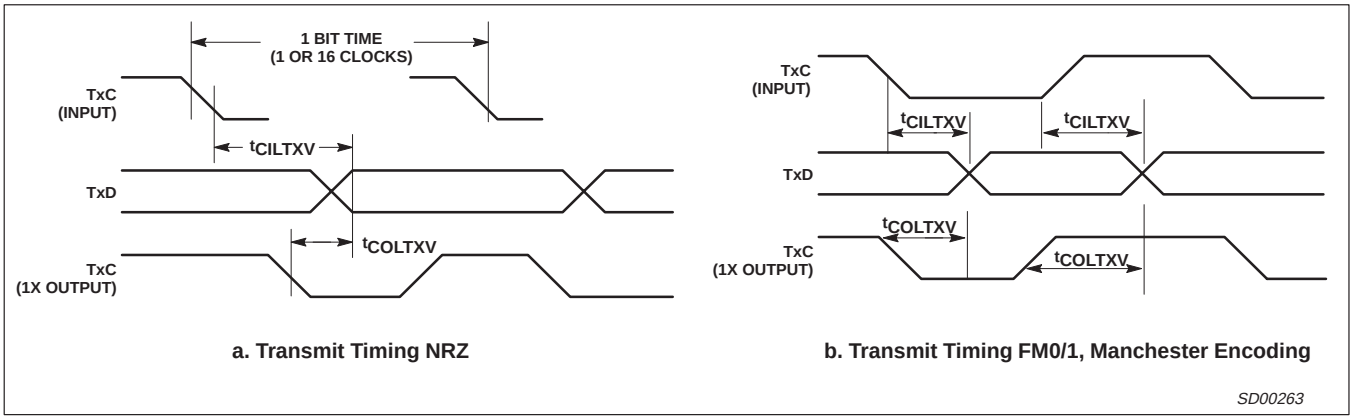


Figure 11.

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{CILTXV}	TxC input LOW (1X) to TxD output (16X) to TxD output	 – –	 120 120	 ns ns
t_{COLTXV}*	TxC output LOW to TxD output (NRZ, NRZI)[9] (FM, Manchester)[9]	 – –	 20 30	 ns ns
NOTE: Characterized with no loads on TxD and TxC outputs.* Tester load approximately 50 pF.				

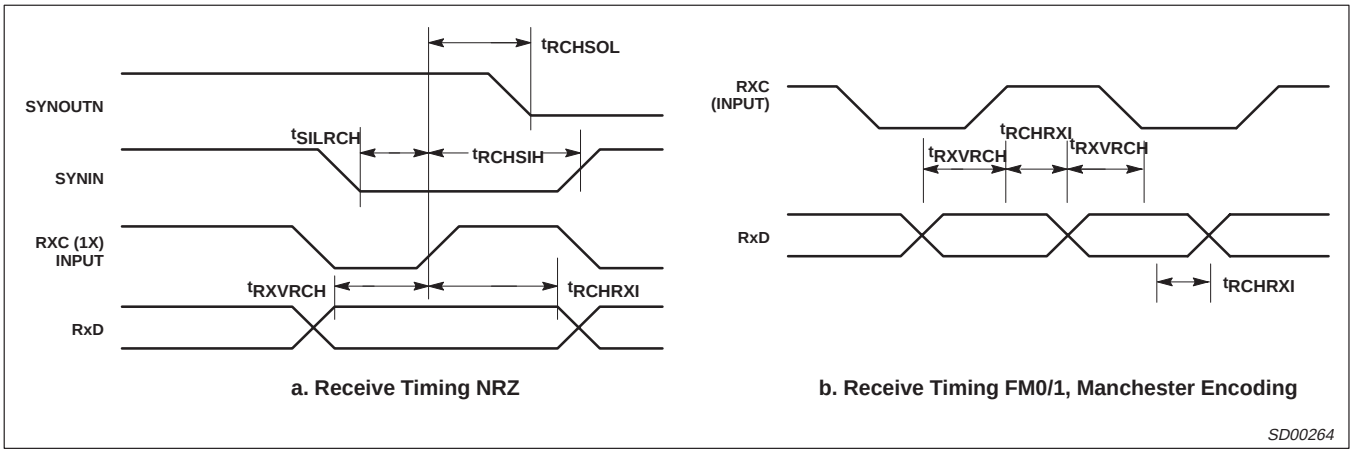


Figure 12.

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RXVRCH}	RxD data valid to RxC HIGH: For NRZ data For NRZI, Manchester, FM0, FM1 data	 20 30	 – –	 ns ns
t_{RCHRXI}	RxC HIGH to RxD data invalid: For NRZ data For NRZI, Manchester, FM0, FM1 data	 20 30	 – –	 ns ns
t_{SILRCH}	SYNIN LOW to RxC HIGH	50	–	ns
t_{RCHSIH}	RxC HIGH to SYNIN HIGH	20	–	ns
t_{RCHSOL}	RxC HIGH to SYNOUT LOW	–	100	ns

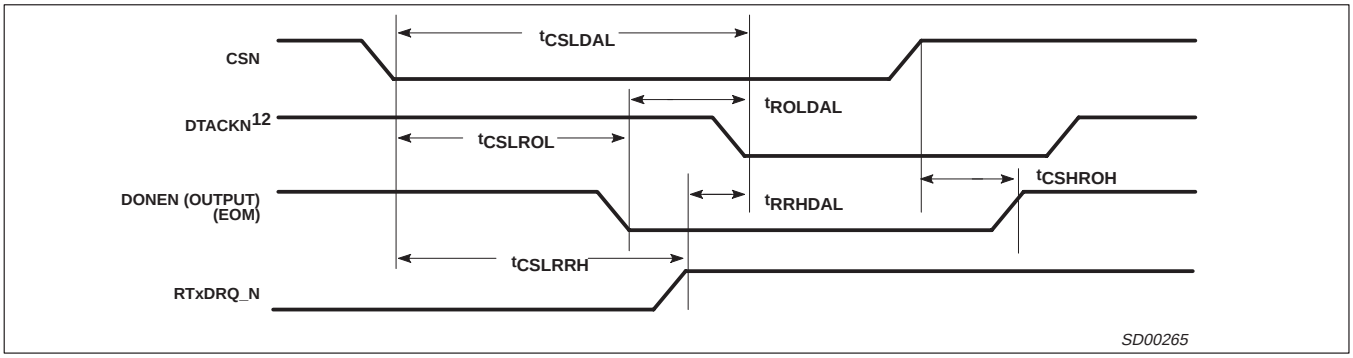


Figure 13. Receive, Dual Address DMA

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{CSLROL}	CSN LOW to Rx DONEN output LOW	–	100	ns
t_{CSLRRH}	CSN LOW to Rx DMA REQN HIGH	–	100	ns
t_{CSHROH}	CSN HIGH to Rx DONEN output HIGH	–	60	ns
t_{ROLDAL}	Rx DONEN output LOW to DTACKN LOW[9]	40	–	ns
t_{RRHDAL}	Rx DMA REQN HIGH to DTACKN LOW[9]	40	–	ns
t_{CSLDAL}[13]	CSN LOW to DTACKN LOW[9]	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns

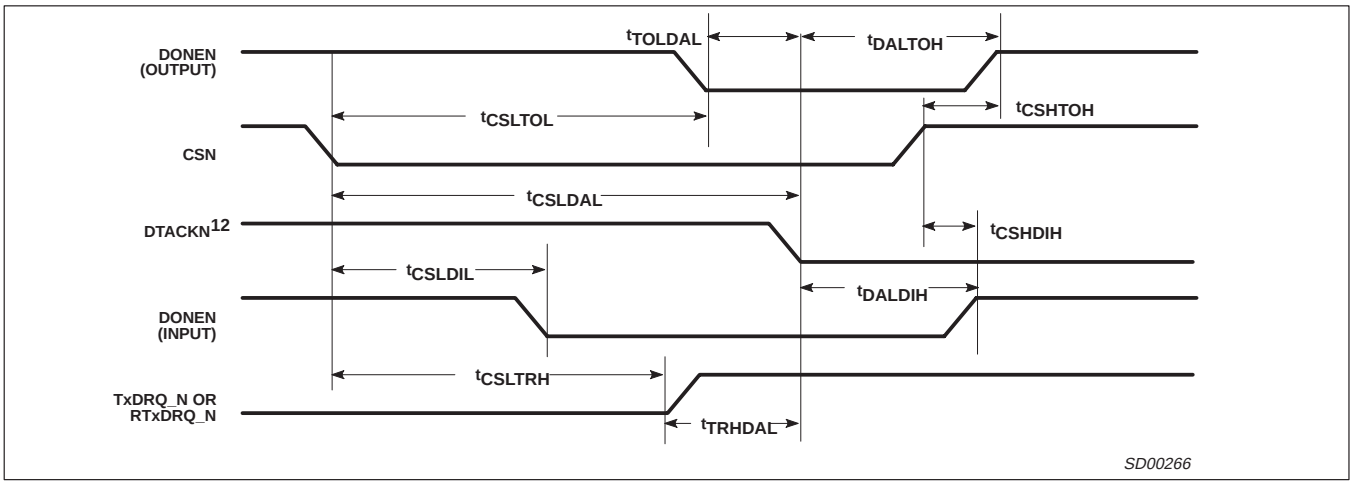


Figure 14. Transmit, Dual Address DMA

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{CSLTOL}	CSN LOW to Tx DONEN output LOW	–	100	ns
t_{CSLTRH}	CSN LOW to Tx DMA REQN HIGH	–	100	ns
t_{DALDIH}	DTACKN LOW to Tx DONEN input HIGH[9]	0	–	ns
t_{DALTOH}	DTACKN LOW to Tx DONEN output HIGH[9]	–	20	ns
t_{TOLDAL}	Tx DONEN output LOW to DTACKN LOW[9]	40	–	ns
t_{TRHDAL}	Tx DMA REQN HIGH to DTACKN LOW[9]	40	–	ns
t_{CSLDAL}[13]	CSN LOW to DTACKN LOW[9]	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{CSLDIL}	CSN LOW to Tx DONEN input LOW	40	–	ns
t_{CSHTOH}	CSN HIGH to Tx DONEN output HIGH	–	60	ns
t_{CSHDIH}	CSN HIGH to Tx DONEN input HIGH	25	–	ns

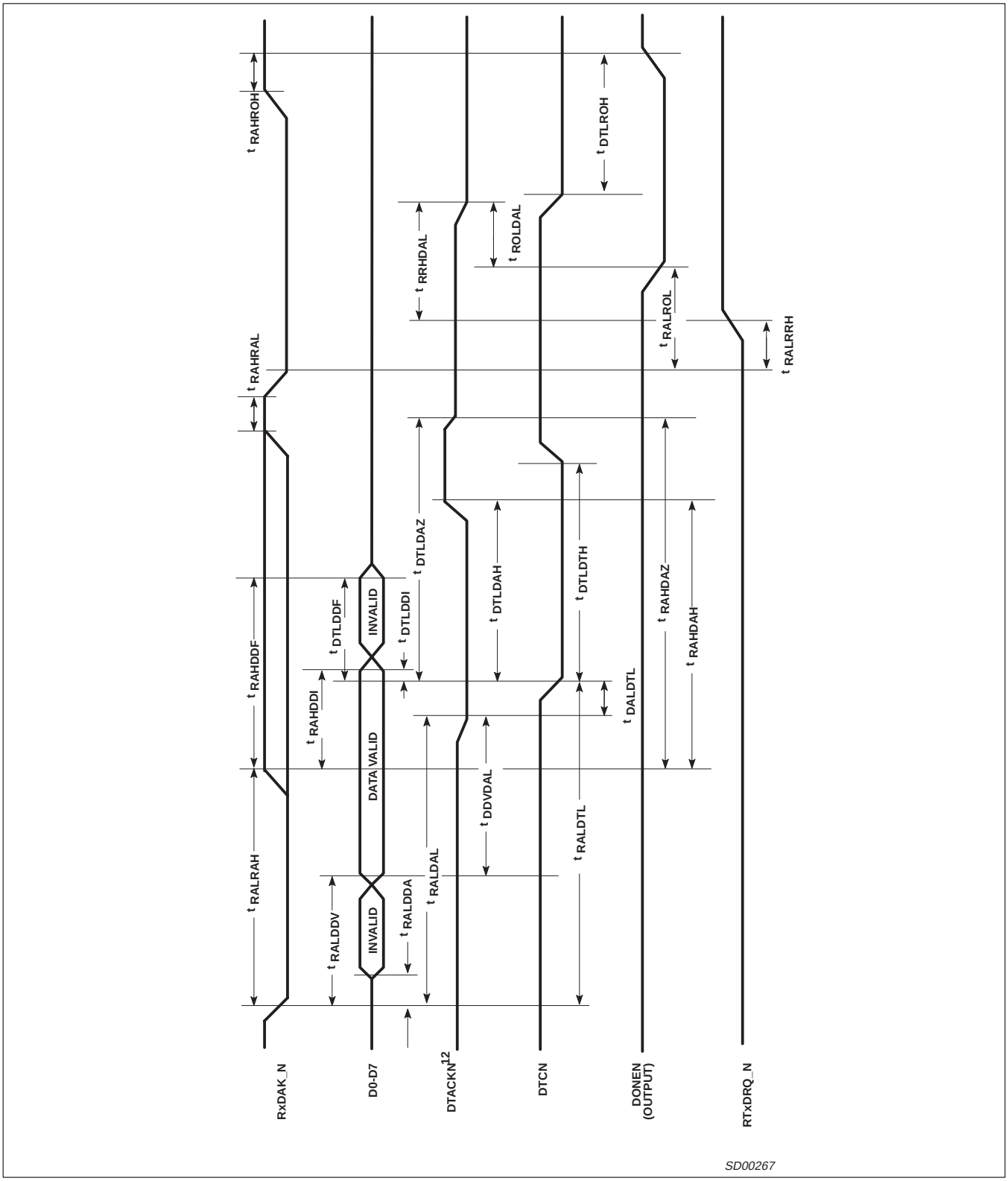


Figure 15. DMA Rx Read Timing—Single Address DMA

DMA Rx Read Timing — Single Address DMA

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RALDDV}	Receive DMA ACKN LOW to read data valid	–	130	ns
t_{DTLDTH}	DTCN LOW to DTCN HIGH	40	–	ns
t_{DALDTL}	DTACKN LOW to DTCN LOW[9]	0	–	ns
t_{DTLDDF}	DTCN LOW to data bus float	–	60	ns
t_{RALDAL}	Rx DMA ACK LOW to DTACKN LOW[9]	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{DDVDAL}	Read data valid to DTACKN LOW[9]	20	–	ns
t_{DTLDAH}	DTCN LOW to DTACKN HIGH	–	80	ns
t_{DTLDAZ}	DTCN LOW to DTACKN high-impedance	–	110	ns
t_{RRHDAL}	Rx DMA REQN HIGH to DTACKN LOW[9]	40	–	ns
t_{ROLDAL}	Rx DONEN output LOW to DTACKN LOW[9]	40	–	ns
t_{RALRRH}	Rx DMA ACKN LOW to receive DMA REQN HIGH	–	100	ns
t_{RAHRAL}	Receive DMA ACKN HIGH to LOW time	30	–	ns
t_{RALROL}	Rx DMA ACK LOW to Rx DONEN output LOW	–	100	ns
t_{DTLROH}	DTCN LOW to Rx DONEN output HIGH	–	70	ns
t_{RALRAH}	Rx DMA ACKN LOW to Rx DMA ACKN HIGH	130	–	ns
t_{RAHDDF}	Rx DMA ACKN HIGH to data bus float	–	60	ns
t_{RALDDA}	Rx DMA ACKN LOW to data bus drivers active[9]	10	–	ns
t_{RAHDDI}	Rx DMA ACKN HIGH to data bus invalid	5	–	ns
t_{DTLDDI}	DTCN LOW to data bus invalid	5	–	ns
t_{RALDTL}	Rx DMA ACKN LOW to DTCN LOW	130	–	ns
t_{RAHDAH}	Rx DMA ACKN HIGH to DTACKN HIGH	–	70	ns
t_{RAHDAZ}	Rx DMA ACKN HIGH to DTACKN high-impedance	–	100	ns
t_{RAHROH}	Rx DMA ACKN HIGH to DONEN output HIGH	–	60	ns

DMA Tx Write Timing — Single Address DMA

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{DTLDTH}	DTCN LOW to DTCN HIGH	40		ns
t_{DALDTL}	DTACKN LOW to DTCN LOW[9]	0		ns
t_{TALDAL}	Tx DMA ACK LOW to DTACKN LOW[9]	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{DTLDAH}	DTCN LOW to DTACKN HIGH		80	ns
t_{DTLDAZ}	DTCN LOW to DTACKN high-impedance		110	ns
t_{TRHDAL}	Tx DMA REQN HIGH to DTACKN LOW[9]	40		ns
t_{TOLDAL}	Tx DONEN output LOW to DTACKN LOW[9]	40		ns
t_{DTLTOH}	DTCN LOW to Tx DONEN output HIGH		70	ns
t_{WDVDTL}	Write data valid to DTCN LOW	40		ns
t_{DTLWDI}	DTCN LOW to write data invalid	20		ns
t_{TALTRH}	Tx DMA ACKN LOW to transmit DMA REQN HIGH		100	ns
t_{TAHTAL}	Transmit DMA ACKN HIGH to LOW time	30		ns
t_{TALTOL}	Tx DMA ACKN LOW to Tx DONEN output LOW		90	ns
t_{DILDTL}	Transmit DONEN input LOW to DTCN LOW	30		ns
t_{DTLDIH}	DTCN LOW to transmit DONEN input HIGH	30		ns
t_{TALTAH}	Tx ACKN LOW to Tx ACKN HIGH	100		ns
t_{TAHWDI}	Tx ACKN HIGH to write data invalid	10		ns
t_{WDVTAH}	Write data valid to Tx DAKN HIGH	40		ns
t_{TAHDAH}	Tx DAKN HIGH to DTACKN HIGH		70	ns
t_{TAHDAZ}	Tx DAKN HIGH to DTACKN HIGH impedance		100	ns
t_{TAHTOH}	Tx DAKN HIGH to DONEN output HIGH		60	ns
t_{DILTAH}	DONEN input LOW to Tx DAKN HIGH	30		ns
t_{TAHDIH}	Tx DAKN HIGH to DONEN input HIGH	25		ns
t_{TALDTL}	Tx DAKN LOW to DTCN LOW	100		ns

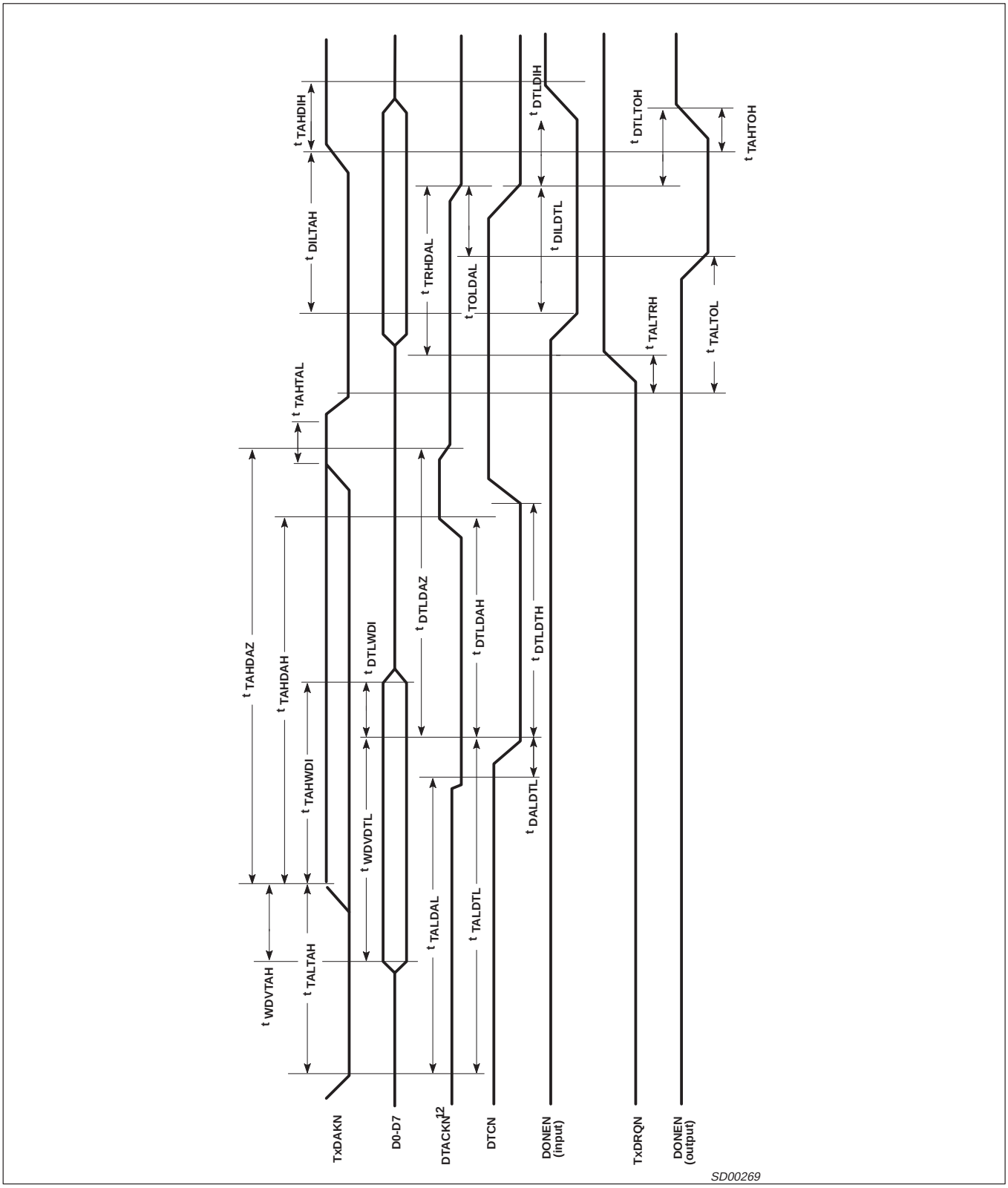


Figure 16. DMA Tx Write Timing—SIngle Address DMA

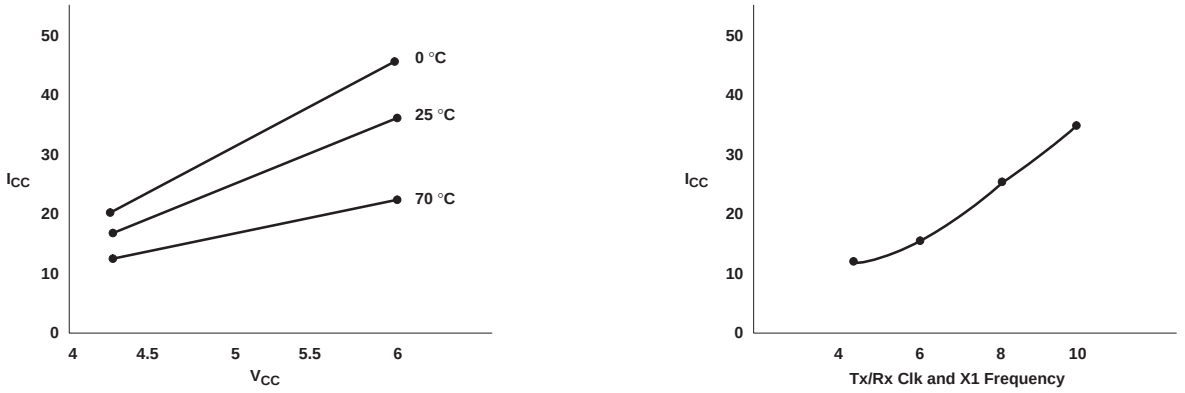


Figure 17.

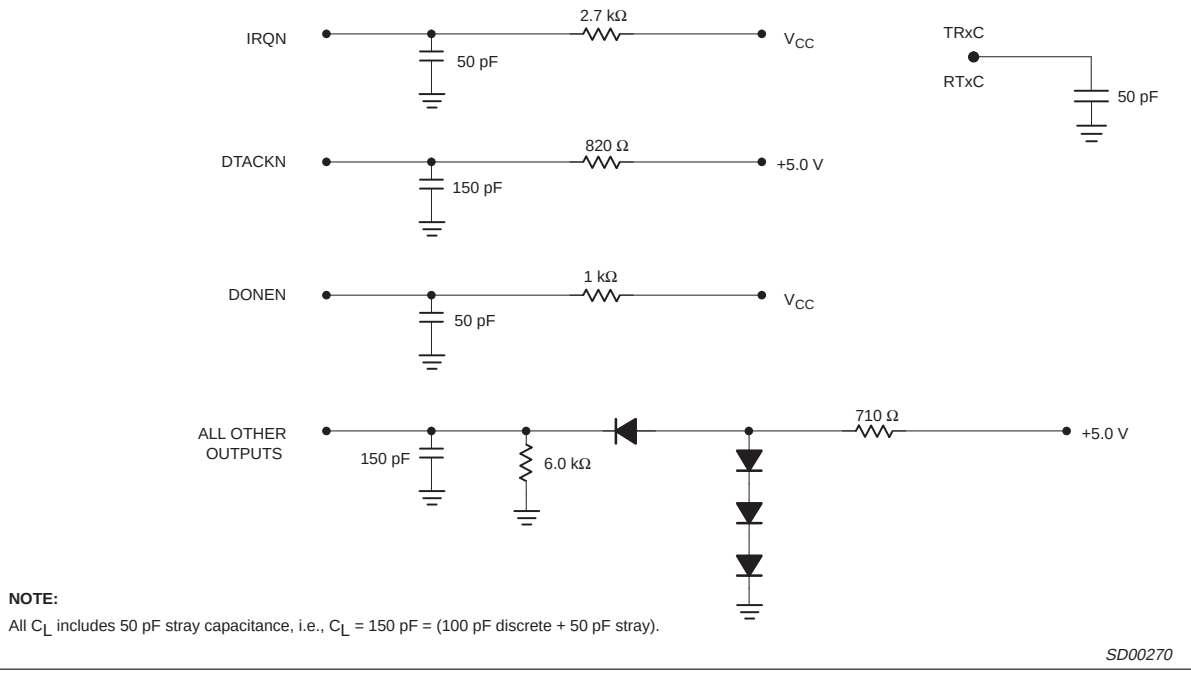


Figure 18. Test Conditions for Outputs

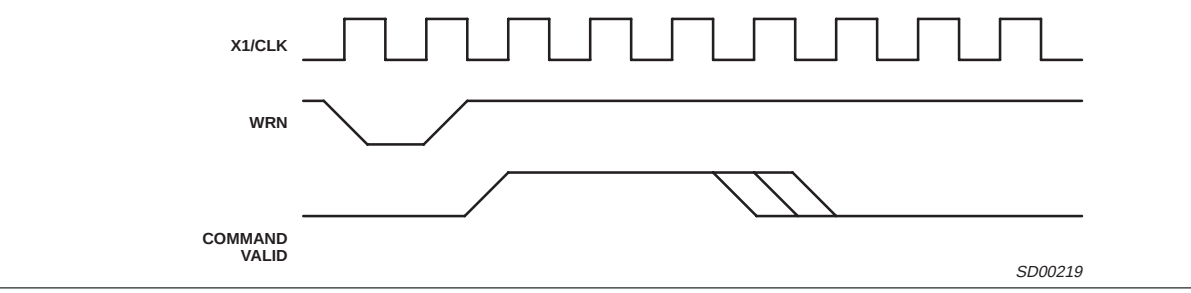


Figure 19. Command Timing

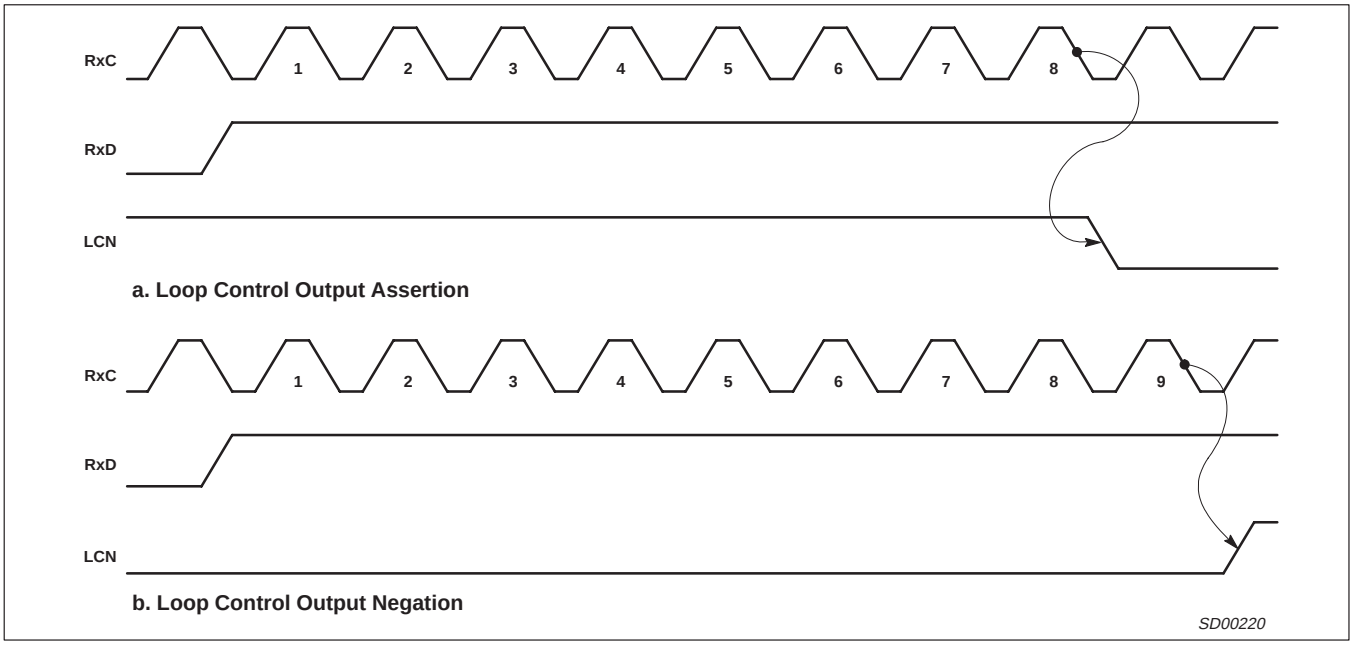


Figure 20. Relationship Between Received Data and the Loop Control Output

REVISION HISTORY

Rev	Date	Description
_3	20040329	**Product data (9397 750 13068). Supersedes data of 1998 Sep 04 (9397 750 04356)** Modifications: ● Remove reference to Type numbers SC68C562C1N and SC68C562A8A (product discontinued), and to “Industrial” temperature range throughout data sheet.
_2	19980904	**Product specification (9397 750 04356). ECN 853-1682 19973 of 04 September 1998. Supersedes data of 1994 Apr 27.**
_1	19940427	

CMOS Dual universal serial communications controller (CDUSCC) SC68C562

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